Remarks

Receipt is acknowledged of the Office Action mailed October 4, 2004. Claims 1-15 were pending in the application. No claims have been amended or cancelled by way of this reply. Thus, claims 1-15 remain pending for reconsideration at this time.

Applicant thanks the Examiner for acknowledging receipt of the priority documentation in the pending application.

Claim Objections

The Office Action Summary indicates in note 7 that claims 1-14 stand objected to. However, no objections are stated in the Office Action. Further, page 3 of the Office Action indicates that claims 1-14 have been allowed. Thus, withdrawal of the objection to claims 1-14 is solicited.

Allowable Subject Matter

Applicant acknowledges with appreciation the allowance of claims 1-14. As no changes have been made to claims 1-14 by way of this reply, claims 1-14 are believed to remain in condition for allowance.

Rejections Under 35 U.S.C. §102(e)

Claim 15 stands rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,526,451 to Kasper ("Kasper" hereafter). Applicant respectfully traverses this rejection for at least the following reasons.

Memory Bus

The Office Action asserts on pages 2-3 that Kasper discloses a memory bus (Fig. 2 [76]) that is configured to transfer data among a plurality of memory devices as presently claimed. Applicant respectfully disagrees. Fig. 2 of Kasper is reproduced below for discussion purposes and for the Examiner's convenience.

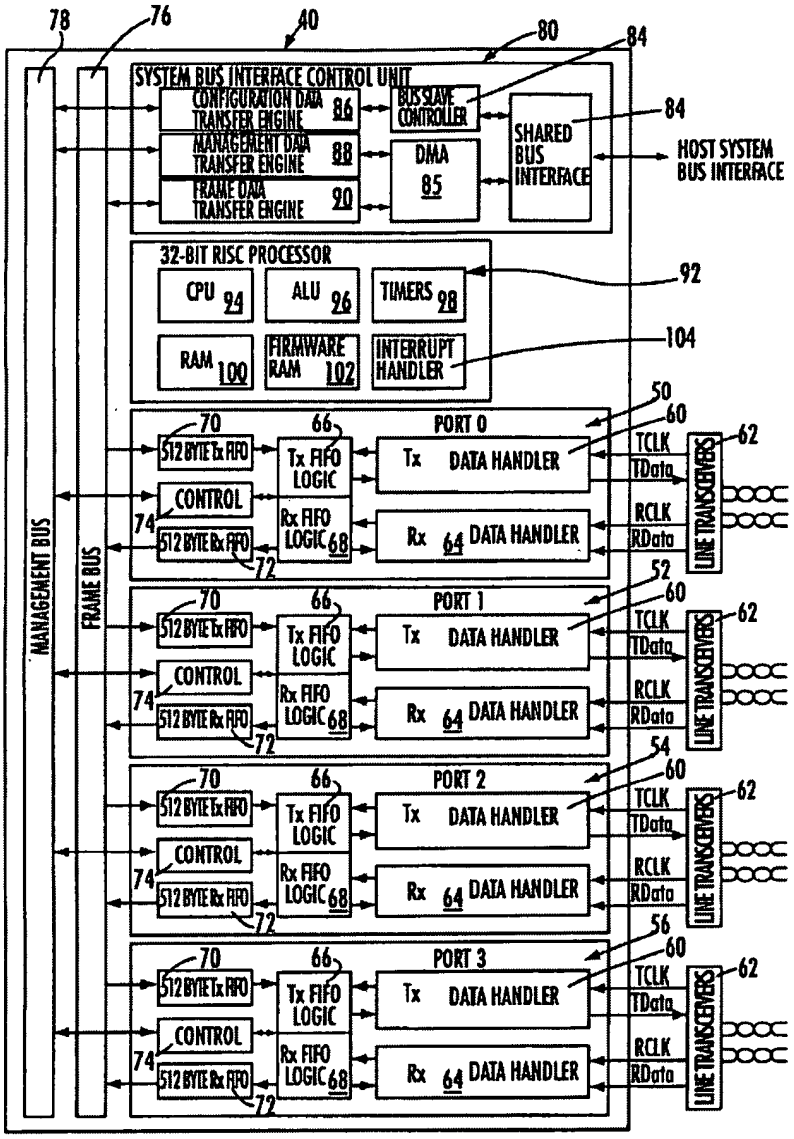


FIG. 2

As shown above, element 76 in Kasper corresponds to FRAME BUS 76. The FRAME BUS 76 in Kasper transmits data between (1) the transmit (Tx) FIFOs 70, receive (Rx) FIFOs 72 and (2) the FRAME DATA TRANSFER ENGINE 90 (col. 6, lines 18-20; lines 37-38) - not between the Tx FIFOs 70 and Rx FIFOs 72 themselves. Such a structure cannot correspond to the claimed memory bus, because claim 15 recites a memory bus configured to transfer data *among the plurality of memory devices* themselves (see pg. 5, lines 8-10 of the as-filed specification) - i.e., not between a plurality of memory devices *and a frame data transfer engine* as disclosed by Kasper. As Kasper fails to disclose or suggest the claimed memory bus, it cannot anticipate claim 15.

External Memory Controller

The Office Action further asserts on pages 2-3 that Kasper discloses a plurality of memory devices (Fig. 2 [70's and 72's]) controlled by an external memory controller (Fig. 2 [80]) to exchange data with an external system bus (Fig. 2 [80] and [HOST SYSTEM BUS INTERFACE]) as presently claimed. Applicant respectfully disagrees.

As shown in Fig. 2 (reproduced above), Kasper discloses an internal CONTROL CIRCUIT 74 that connects each Tx FIFO 70 and Rx FIFO 72 pair to the internal MANAGEMENT BUS 78 and controls their access thereto (col. 6, lines 18-23). Further, Kasper discloses an internal SYSTEM BUS INTERFACE CONTROL UNIT 80 that functions as the interface between the internal MANAGEMENT BUS 78 of the system and the HOST SYSTEM BUS INTERFACE. Such a structure does not correspond to the structure presently recited in claim 15.

In order to more fully illustrate differences with Kasper and for the Examiner's convenience, Fig. 4 of the as-filed specification is reproduced below.

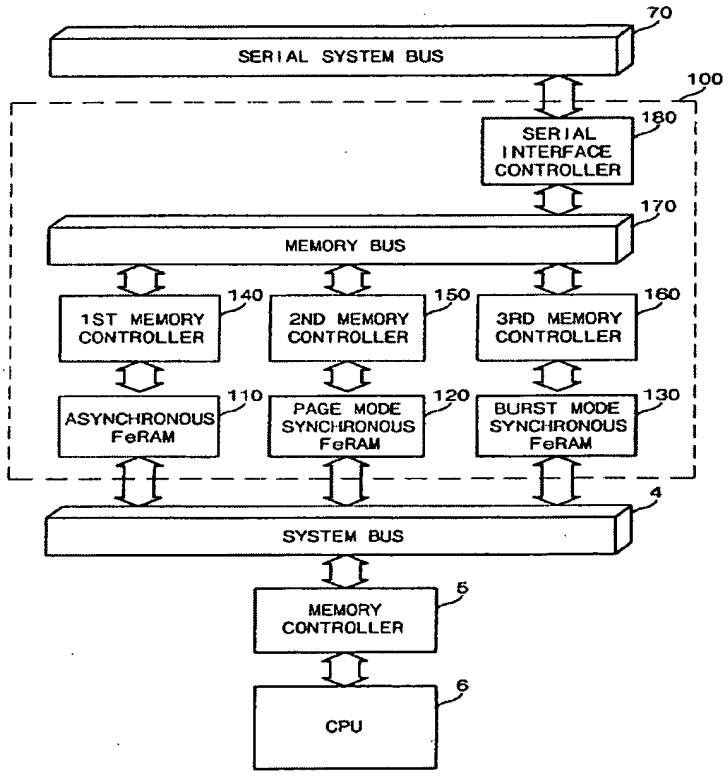


Fig.4

As shown above, the system includes an external MEMORY CONTROLLER 5 that controls data exchange with external SYSTEM BUS 4. These components are considered to be *external* because they are located outside of composite memory device 100. Similarly, the memory bus 170 and controllers 140, 150, 160 and 180 are considered to be *internal* because they are located within composite memory device 100. Due to the depicted structure, when one of the plurality of memory devices, for example FeRAM 100, interfaces with the external SYSTEM BUS 4 controlled by the external MEMORY CONTROLLER 5, the rest memory devices 120, 130 are allowed to exchange data via internal MEMORY BUS 170 controlled by internal CONTROLLERs 150, 160 respectively.

Hence, it should be appreciated that, unlike Kasper, the claimed *external* MEMORY CONTROLLER 5 and *external* SYSTEM BUS 4 are located outside of the composite memory device 100 - they do not correspond to the SERIAL INTERFACE CONTROLLER 180 and SERIAL SYSTEM BUS 70, which are *internal* to the composite memory device 100. As Kasper fails to disclose or suggest the claimed *external* memory controller and *external* memory bus, it cannot anticipate claim 15 for this additional reason.

Rest memory devices

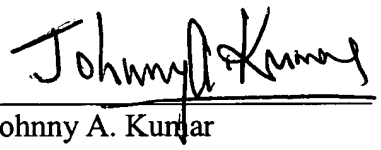
The Office Action also asserts on pages 2-3 that Kasper discloses when one of the plurality of memory devices (Fig. 2 [70 and 72] of port 0) exchanges data with the external system bus (Fig. 2 [80]), the rest memory devices (Fig. 2 [70 and 72] of ports 1-3) are allowed to exchange data via the memory bus (Fig. 2 [76]). Applicant respectfully disagrees.

As shown in Fig. 2, the FRAME BUS 76 in Kasper is connected with the HOST SYSTEM BUS INTERFACE via the SYSTEM BUS INTERFACE CONTROL UNIT 80. Accordingly, when a Tx FIFO 70 or Rx FIFO 72 exchanges data with the HOST SYSTEM BUS INTERFACE, the FRAME BUS 76 is occupied by the SYSTEM BUS INTERFACE CONTROL UNIT 80 such that the FRAME BUS 76 cannot be used for internal data exchange between the rest Tx FIFOS 70 or Rx FIFOs 72. Thus, Kasper cannot operate in the manner asserted by the Office Action, and fails to anticipate claim 15 for this additional reason.

CONCLUSION

In view of the above remarks, Applicant respectfully requests that all objections and rejections be withdrawn and that a notice of allowance be forthcoming. The Examiner is invited to contact the undersigned for any reason related to the advancement of this case.

Respectfully submitted,



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Johnny A. Kumar
Attorney for Applicant
Reg. No.: 34,649

Heller Ehrman White & McAuliffe LLP
1666 K Street, N.W., Suite 300
Washington, D.C. 20006-4004
Telephone: (202) 912-2000
Facsimile: (202) 912-2020

Customer No. 26633